## REMARKS

Claims 17-22 are pending and have been rejected on the basis of obviousness-type double patenting and under Section 102 in view of the Uchiyama reference (USP 6,748,507).

Initially, Applicant notes that it has amended independent claim 17 to clarify the intended scope of the claimed invention. Namely, the data processor operates in a plurality of modes, and the operating mode in which the data processor operates is based on the mode register. See, e.g., Fig. 4 of the specification and related description in the specification, and in particular standby control register STBYR. In accordance with the present invention, the operation mode may be controlled based on contents of the mode register. The operation modes include a first operation mode (CPU executes instructions), a second operation mode (CPU and clock pulse generator halt operation), and a third operation mode (CPU halts executing instructions and clock pulse generator generates clock signals). The combination of elements and features recited in claim 17 (e.g., central processing unit, clock pulse generators, the recited modes, etc.) patentably distinguish Applicant's invention from the cited references.

As for the double patenting rejection, Applicant respectfully traverses this rejection. USP 6,748,507 claims inventions related to a single chip microcomputer/data processor and control of access to external memory. These inventions, respectfully, are patentably distinct over the presently claimed invention, which is directed to controlling modes of operation of the data processors such as recited in claim 17. Accordingly, Applicant submits that the double patenting rejection should be withdrawn.

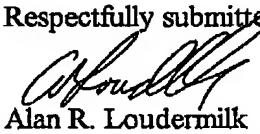
As for the rejection in view of Uchiyama, particularly in view of the invention recited in the claims as presented herein, Applicant respectfully submits that this rejection should be withdrawn. Uchiyama relates to a processing system including an MPU and synchronous DRAM. A mode register is provided (CMR 505) as noted by the Examiner, but this register relates to controlling the operation of the synchronous DRAM. This mode register does not, however, control operation of the MPU, and this reference does not disclose or suggest Applicant's invention. Accordingly, Applicant submits that its invention, as defined in the presently pending claims, patentably distinguishes over Uchiyama and the other cited references.

If there are any questions or issues regarding the foregoing, Applicant requests an opportunity to discuss such matters with the Examiner by way of an in-person or telephone interview.

Please charge any additional fees due, or credit any overpayment, to Deposit Account No. 50-0251.

No new matter has been added.

Respectfully submitted,



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